IN THE CLAIMS

1. (Currently amended) A method for forming a semiconductor device on a semiconductor substrate, the method comprising:

(a) forming isolation layers that define a memory cell area and a peripheral circuit area on the semiconductor substrate and isolate each ~~device~~ area;

(b) forming a first conductive type transistor in the memory cell area and a first conductive type transistor and a second conductive type transistor in the peripheral circuit area, each transistor including source/drain regions, a gate electrode having sidewall spacers, and a first etch stopping layer;

(c) forming an interlayer insulating ~~layers~~ layer overlying the first and second conductive type transistors;

(d) ~~removing portions of the interlayer insulating layer to form openings that expose the source/drain regions of the transistors in the memory cell area and the peripheral circuit area, and filling the openings with a conductive material~~

exposing the source/drain regions of the first conductive type transistor in the memory cell area and the peripheral circuit area by etching the interlayer insulating layer;

forming first conductive type polysilicon layers on the exposed source/drain regions of the first conductive type transistors;

thereafter, exposing the source/drain regions of the second conductive type transistor in the peripheral circuit area by etching the interlayer insulating layer; and

forming a second conductive type polysilicon layer on the exposed source/drain regions of the second conductive type transistor; and

(e) concurrently forming contact pads on the source/drain regions in the memory cell area and the source/drain regions in the peripheral circuit area.

2. (Original) The method of claim 1, wherein the conductive material is doped polysilicon.

3. (Cancelled)

4. (Original) The method of claim 1, further comprising forming a second etch stopping layer overlying the transistors after (b).

5. (Original) The method of claim 4, wherein the second etch stopping layer has lower etching selectivity than the interlayer insulating layer in (d).

6. (Original) The method of claim 5, wherein the second etch stopping layer is a silicon nitride layer.

7. (Currently amended) The method of claim 1, wherein (e) comprises etching back the conductive material in the memory cell area and the peripheral circuit area, and etching back the interlayer insulating ~~layers~~ layer in the memory cell area and the peripheral circuit area.

8. (Original) The method of claim 1, wherein in (e) comprises chemical mechanical polishing the conductive material and the interlayer insulating layer.

9. (Currently amended) A method for forming a semiconductor device, comprising:

(a) forming isolation layers for defining a memory cell area and a peripheral circuit area on a semiconductor substrate and isolating each ~~device~~ area;

(b) forming a first conductive type transistor in the memory cell area and a first conductive type transistor and a second conductive type transistor in the peripheral circuit area by forming source/drain regions and gate electrodes having sidewall spacers, and first etch stopping layers in the memory cell area and the peripheral circuit area of the semiconductor substrate;

(c) forming conductive epitaxial layers, which extend from the source/drain regions onto the isolation layers, on the respective source/drain regions;

(d) forming an interlayer insulating layer overlying the transistors and the conductive epitaxial layers;

(e) forming plugs by patterning the interlayer insulating layer, and forming openings in the interlayer insulating layer to expose ~~opening~~ the source/drain regions of the transistors in the memory cell area and the peripheral circuit area, and filling the openings with metal; and

(f) concurrently forming metal contact pads in the memory cell area and the peripheral circuit area.

10. (Currently amended) The method of claim 9, wherein step (c) comprises:

forming conductive epitaxial layers on the source/drain regions of the semiconductor substrate;

implanting first conductive type impurity ions by forming a photoresist pattern for opening the conductive epitaxial layers formed on the source/drain regions of the first conductive type transistor and then using the photoresist pattern as an implantation mask; and

implanting second conductive type impurity ions by forming a photoresist pattern for opening the conductive epitaxial layers formed on the source/drain regions of the second conductive type transistor and then using the photoresist pattern as an implantation mask.

11. (Currently amended) The method of claim 10, wherein ~~the~~ a doping concentration of the conductive epitaxial layers is $10^{19} \sim 10^{21}$ atoms/cm^3.

12. (Currently amended) The method of claim 9, wherein the conductive epitaxial layers comprise silicon.

13. (Currently amended) The method of claim 10, wherein the conductive epitaxial layers comprise silicon.

14. (Currently amended) The method of claim 9, wherein node-separation in (f) is performed by etching back or chemically and mechanically polishing the conductive metal plugs and the interlayer insulating ~~layers~~ layer.

15. (Original) The method of claim 9, wherein the metal in (e) is tungsten.

16. (Currently amended) A method of forming a semiconductor device having metal contact pads on source/drain regions of transistors in a peripheral circuit area for writing and reading data in memory cells on a semiconductor substrate, the method comprising:

(a) forming first and second gate electrodes having sidewall spacers and etch stopping layers in the peripheral circuit area;

(b) forming an interlayer insulating layer overlying the first and second gate electrodes;

(c) forming first and second conductive type transistors by forming an opening in portions of the interlayer insulating layer on ~~the~~ an active area including the first and second gate electrodes, implanting first and second conductive type impurities into the opening, and forming source/drain regions;

(d) forming a metal layer in the opening; and

(e) forming metal contact pads by node-separating the metal layer.

17. (Currently amended) The method of claim 16, wherein ~~the~~ a concentration of the first and second conductive type impurities is $10^{19} \sim 10^{21}$ atoms/cm^3.

18. (Original) The method of claim 16, wherein (c) comprises:

forming a first opening by etching a portion of the interlayer insulating layer on the active area including the first gate electrode;

forming a first conductive type source/drain region on the semiconductor substrate by implanting first conductive type impurities into the first opening;

forming a second opening by etching a portion of the interlayer insulating layer on the active area including the second gate electrode; and

forming a second conductive type source/drain region on the semiconductor substrate by implanting second conductive type impurities into the second opening.

19. (Original) The method of claim 16, wherein (c) comprises:

etching a portion of the interlayer insulating layer on the active areas each including the first and second gate electrodes;

forming a first conductive type source/drain region by implanting first conductive type impurities into the active area including the first gate electrode in the opening; and

forming a second conductive type source/drain region by implanting second conductive impurities into the active area including the second gate electrode in the opening.

20. (Currently amended) The method of claim 16, wherein in the opening of (c), the interlayer insulating layer on a non-active area between the first and second gate electrodes is removed so that the source/drain ~~region~~ regions of the first conductive type transistor is locally connected to the source/drain region of the second conductive type transistor by the metal contact pads which are node-separated.

21. (Currently amended) A method of forming a semiconductor device including a memory cell area having a plurality of memory cells and a peripheral circuit area for writing and reading data in the memory cells in the memory cell area of a semiconductor substrate, the method comprising:

(a) forming isolation layers for defining a memory cell area and a peripheral circuit area on the semiconductor substrate and isolating each ~~device~~ area;

(b) forming a first conductive type transistor in the memory cell area and a first conductive type transistor and a second conductive type transistor in the peripheral circuit area by forming source/drain regions and gate electrodes having sidewall spacers, and first etch stopping layers in the memory cell area and the peripheral circuit area of the semiconductor substrate;

(c) forming a first insulating layer overlying the transistors;

(d) forming plugs by patterning the insulating layer, forming openings in the first insulating layer to expose the source/drain regions of the transistors in the memory cell area and the peripheral circuit area, and filling the openings with a conductive material;

(e) forming contact pads on the source/drain regions in the memory cell area and the source/drain regions in the peripheral circuit area, concurrently by etching the first insulating layer and the plugs and then node-separating the plugs;

forming a second etch stopping layer on the contact pads;

(f) forming a second insulating layer on the contact pads with the second etch stopping layer; and

(g) forming a contact plug on at least one contact pad.

22. (Cancelled)

23. (Currently amended) The method of claim ~~22~~ 21, wherein the second etch stopping layer has lower etching selectivity than the second insulating layer.

24. (New) A method for forming a semiconductor device on a semiconductor substrate, the method comprising:

forming isolation layers that define a memory cell area and a peripheral circuit area on the semiconductor substrate and isolate each area;

forming a first conductive type transistor in the memory cell area and a first conductive type transistor and a second conductive type transistor in the peripheral circuit

area, each transistor including source/drain regions, a gate electrode having sidewall spacers, and an etch stopping layer;

forming an interlayer insulating layer overlying the first and second conductive type transistors;

etching the interlayer insulating layer to expose the source/drain regions of the first conductive type transistor in the memory cell area and the peripheral circuit area by;

forming first conductive type polysilicon layers on the exposed source/drain regions of the first conductive type transistors;

thereafter, etching the interlayer insulating layer to expose the source/drain regions of the second conductive type transistor in the peripheral circuit area; and

forming a second conductive type polysilicon layer on the exposed source/drain regions of the second conductive type transistor; and

etching back the interlayer insulating layer to form contact pads concurrently on the source/drain regions in the memory cell area and on the source/drain regions in the peripheral circuit area.

25. (New) The method of claim 24, further comprising forming a second etch stopping layer overlying the transistors after (b).

26. (New) The method of claim 24, wherein the second etch stopping layer has lower etching selectivity than the interlayer insulating layer in (d).